(Pages : 3) **N – 5776**

Reg. No. .....

Name : .....

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**Eighth Semester B.Tech. Degree Examination, April 2022**

**13.802 – COMPUTER SYSTEM ARCHITECTURE (R)**

**(2013 Scheme)**

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. Compare CISC and RISC architectures.
2. Explain the routing functions in Barrel shifter networks
3. Compare and contrast linear and non-linear pipelining.
4. Compare implicit and explicit forms of parallelism.
5. What do you mean by cache coherency? Explain.

**(5 × 4 = 20 Marks)**

PART – B

Answer **one** full question from each module.

**Module I**

6. (a) Explain the properties of an interconnection network. **8**

   (b) Explain the following w.r.t a linear pipeline (i) Speedup (ii) Efficiency and (iii) Throughput. **12**

OR

P.T.O.

7. (a) Explain the concept of reservation tables with an example pipeline. 8

(b) With block diagrams, explain Flynn's classification. 12

## Module II

8. (a) Explain fetch and main memory update policies applied to cache memory. 8

(b) Consider a two-level memory system with four page frames. A certain program generated the following page trace: 0,1,3,6,2,4,5,2,5,0,3,1,2,5,4,1,0.

(i) Find out the allotment of pages to the four page frames using LRU, OPT and FIFO page replacement policies.

(ii) Compare the hit ratios associated with each of the three replacement policies. 12

OR

9. (a) Compare and contrast placement policies in cache memory. 10

(b) Explain program relocation and program locality. 10

## Module III

10. (a) Explain S access and C access memory organizations. 10

(b) Explain how two floating point numbers can be added using a pipelined processor. 10

OR

11. (a) What are the different types of data dependent hazards? How these hazards can be avoided? 12

(b) Explain classification of pipelined processors. 8

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## Module IV

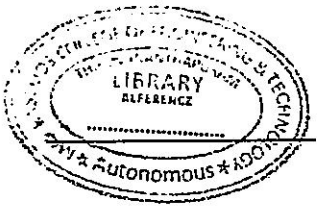
12. (a) With a block diagram explain the components of a Processing Element (PE). **5**

    (b) Explain working of an SIMD machine with an example. **15**

OR

13. (a) Explain (i) Data flow architecture and (ii) Hybrid architecture. **12**

    (b) Explain Intel paragon system architecture. **8**




**(4 × 20 = 80 Marks)**