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Reg. No. .....

Name : .....

Eighth Semester B.Tech Degree Examination, May 2022

(2008 Scheme)

08.802 COMPUTER SYSTEM ARCHITECTURE (R)

Time : 3 Hours Max. Marks : 100

PART-A

Answer **ALL** questions

1. A benchmark Program with 50000 Integer, 40000 Data Transfer, 10000 Floating Point and 8000 Control Instructions is executed on a 100MHz processor. The instructions require 1,2,2, and 2 clock cycles respectively for execution. Calculate the CPI, MIPS and Execution Time of the benchmark.

2. Explain the Omega and Crossbar interconnect network.

3. Explain the detection of parallelism with Bernstein's conditions. Is this an efficient technique? Justify.

4. Consider a two-level memory hierarchy M_1 and M_2 with access times t_1 and t_2, cost per byte c_1 and c_2, and capacities s_1 and s_2 respectively. The first level memory hit ratio h=0.9. Calculate the effective access time E of this memory system. Also find out the total cost of the memory system.

5. What are the design trade-offs between large register files and large D-Cache?

6. Compare the pipelining in vector processors and scalar processors. What are the limiting factors of degree of superscalar design?

P.T.O.

7. A non-pipelined processor P_1 has clock rate of 100 MHz and an average CPI of 4. P_1 is improved to P_2 as a pipelined processor with 5-stage linear instruction pipeline and reduced clock rate of 80 MHz (due to latch delay). What is the speedup at P_2 over P_1 if a program with 400 instructions is executed. Also find the MIPS of both processors.

8. Explain the Write-Once cache coherence protocol.

9. Explain S-access, C-access and C/S-access memory organizations for vetor accesses.

10. What are the context switching policies in multi threaded architectures?

(10 × 4 = 40 Marks)

PART-B

Answer any **ONE** full question from each module.

Module I

11. Describe Parallel Random-Access Model and the variants. Explain any one of the variant in the context of an n x n matrix multiplicaiton. Discuss the time complexity. **(20)**

OR

12. (a) Write a note on the Data-Routing Function in interconnect. **(8)**

    (b) Compare the Multi-Processor, Message-Passing, Multi Vector and SIMD architectural models. **(12)**

Module II

13. (a) Explain the collision free scheduling with an example. **(10)**

    (b) With a neat diagram explain the address translation with TLB. **(10)**

OR

14. Explain the superscalar pipeline design in detail. Explain the in-order and out-of-order issue of instructions with an example. **(20)**

Module III

15. (a) Explain the performance-directed design goals of super computers. Use examples wherever possible. **(10)**

(b) With a note on the six common types of vector instructions. **(10)**

OR

16. Explain the prefetching and relaxed memory put space consistency models for hiding latency in MPPs. **(20)**

(3 × 20 = 60 Marks)