(Pages : 2)

L – 6112

Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, May 2021

(2008 Scheme)

08.306 : DIGITAL ELECTRONICS (T)

Time : 3 Hours

Max. Marks : 100

PART – A

Answer all questions. Each question carries 4 marks.

1. State and prove De Morgan 's Theorem.
2. Write VHDL program for NOR and NAND gate.
3. Design a half adder circuit and realize using NAND gates only.
4. Realise a full adder using the 3x8 decoder.
5. Compare the characteristics of TTL and CMOS logic families.
6. Realise a full adder using two half adders.
7. Draw the truth – table and logic circuit diagram of a ring counter.
8. How can a 74121 be configured as a monostable multivibrator for a described pulse width?
9. Distinguish between sequential and combinational circuits.
10. What is the difference between a Moore amid Mealy machines? Explain with examples.

(10 x 4 = 40 Marks)

P.T.O.

PART – B

Answer **any two** from the module. Each question carries 10 marks.

Module – I

11. Simplify the following Boolean expression using K–Map and realize it using NAND gate unit.

$F(A,B,C,D) = \Sigma m(1,4,9,10,11,12,14) + \Sigma d(0,8,13)$

12. Design a 4 bit Carry look ahead adder.

13. (a) Write the VHDL code for the implementation of a full adder circuit.

(b) Compare static RAM and dynamic RAM.

Module – II

14. Explain the operation of a Master slave JK flip-flop. What is meant by race around condition?

15. Explain the working of Universal Shift Register.

16. Draw a neat diagram of TTL NAND gate and explain its Operation. What is meant by sourcing and sinking?

Module – III

17. (a) What are races and cycles with examples.

(b) Explain static, dynamic and essential hazards with examples.

18. Design a mode 6 Up-Down counter using state table and state diagram.

19. Design a sequence detector to detect a sequence '101101' in a stream of bits.

(3 × 20 = 60 Marks)

S3_ EC_ 2008 Sch.

2021 Ktu