(Pages : 2) **K – 4286**

Reg. No. : .....

Name : .....

Fourth Semester B.Tech. Degree Examination, September 2020

13.402 — COMPUTER ORGANIZATION AND DESIGN (FR)

(2013 Scheme)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. Register R1 and R1 contain the decimal values 1200 and 2400.What is the effective address's (EA) of memory operand in each of the following?

   (a) Load 20(R1), R5

   (b) Add – (RI), R5

   (c) Mov #3000, R5 and

   (d) Sub (R1)+, R5

2. Discuss flash memory.

3. What will be the width of address and data bus for a 512kX8 memory chip?

4. Describe the memory hierarchy.

5. What are the difference between subroutine and interrupt service routine?

(5 × 4 = 20 Marks)

P.T.O.

PART – B

Answer **any one** questions from **each** Module.

Module – I

6. (a) Draw and explain the basic diagram of a simple computer with functional units. **(10)**

   (b) Explain the difference between CISC and RISC. **(10)**

7. (a) What are the techniques used to measure the performance of a computer? **(10)**

   (b) Illustrate the different classes of instruction formats with example. **(10)**

Module – II

8. (a) Design the five stage organization with multiplexer and inter-stage register and explain each stage. **(10)**

   (b) Explain the execution of a computer instruction with example. **(10)**

9. (a) Design arithmetic and logic unit and explain in detail. **(10)**

   (b) Illustrate the conditional control statement with example. **(10)**

Module – III

10. Explain micro program sequencer with neat diagram. **(20)**

11. (a) Distinguish between horizontal and vertical micro instruction. Discuss advantages and disadvantages of each scheme. **(10)**

    (b) Explain an organization of CUP with Hardwired control unit **(10)**

Module – IV

12. (a) Illustrate the implementation of an output interface for a display device. Explain the functions of each signal handled by interface. **(10)**

    (b) Elucidate the concepts of Direct Memory Access. **(10)**

13. (a) Draw the timing diagram for write operation on the PCI. **(10)**

    (b) Describe the organization of a 2M × 32 memory module using 512K × 8 static memory chip. **(10)**
