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J – 4699

Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, May 2020

(2013 Scheme)

13.306 : DIGITAL ELECTRONICS (T)

Time : 3 Hours

Max. Marks : 100

PART – A

Answer **all** questions. Each carry **2** marks.

1. Convert $A0F9.0EB_{16}$ to decimal.
2. Reduce expression $f = A + B\left[AC + \left(B + \overline{C}\right)D\right]$
3. Draw the circuit of a half subtracter with help of truth table.
4. Explain toggle effect in JK flip flop.
5. Draw the circuit of a 3 bit Johnson counter using D flip flop.
6. Draw the circuit of a 2 bit ripple up Asynchronous counter using JK flip flop.
7. What are the differences between Moore and Mealy circuits. Draw their state diagrams.
8. What are the differences between synchronous and asynchronous sequential circuit.
9. Explain working of CMOS inverter.
10. Write short note on PROM.

P.T.O.

PART – B

Answer **any one** question from **each** Module. Each full question carries **20** marks.

Module – I

11. Reduce using K-map the expression $f = \prod M\,(2, 8, 9, 10, 11, 12, 14)$ and implement the real minimal expression using NOR gate.

12. Explain the working of a multiplexer and implement $F = \sum m(1, 2, 4, 7)$ using an 4:1 MUX.

Module – II

13. Design a synchronous mode 6 counter with JK flip flops.

14. Design an astable multivibrator using 555 timer to generate a square wave of frequency 5 KHz with 70% duty cycle and explain its working with the internal diagram.

Module – III

15. Draw the state diagram and state table of D and T flip flops for Mealy model.

16. Draw the state diagram and the state table for a Moore type sequence detector to detect the sequence 1010.

Module – IV

17. With neat circuit diagram explain the working of CMOS inverter and CMOS NAND gate.

18. With help of neat diagram explain the working of TTL NAND gate circuit. Also explain the advantages and disadvantages of totem-pole arrangement.
