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Reg. No : .....

Name : .....

Eighth Semester B.Tech. Degree Examination, November 2019

(2013 Scheme)

13.802 : COMPUTER SYSTEM ARCHITECTURE (R)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. Each question carries **4** marks.

1. Discuss briefly about Flynn's classification of computer architecture.
2. What is the significance of Bernsteins's condition in determining parallelism in programs?
3. Differentiate between synchronous and asynchronous model of linear pipline processors.
4. Briefly describe cache coherence problems.
5. Distinguish between static and dynamic dataflow computers.

(5 × 4 = 20 Marks)

PART – B

Answer **all** questions.

Module – I

6. (a) Explain the various parameters used for evaluation of system performance. Write its significance. **5**

(b) Explain the differences between UMA, NUMA, COMA model with neat diagram. **15**

OR

P.T.O.

7. (a) What are the different types of data, control and structural hazards pipelined processors. How these hazards can be resolved? **15**

(b) Describe briefly about operational model of SIMD computers with an example. **5**

Module – II

8. (a) Explain the importance of memory hierarchy. How the performance of a memory hierarchy is determined? **10**

(b) What are the different types of interleaved memory organization and it advantage? **10**

OR

9. (a) Explain the different types of vector architecture. **10**

(b) Write a note on VLIW processors and its pipeline operation. **10**

Module – III

10. (a) Consider the following reservation table for four stage pipeline with clock cycle =20 ns. **15**

(i) What are the forbidden latencies and the initial collision vector?

(ii) Draw the state transition diagram.

(iii) Determine the MAL associated with the greedy cycle.

(iv) Determine the pipeline throughput corresponding to the MAL.

(v) Determine the lower bound on the MAL for this pipeline.

X					X
	X		X		
		X			
			X	X	

(b) Define (i) speedup (ii) efficiency (iii) throughput of a processor pipline. **5**

OR

11. (a) Explain the mechanism for instruction pipelining. **10**

(b) Explain Tomasulo's algorithm for dynamic instruction scheduling. **10**

Module – IV

12. (a) Explain blocking and non blocking network with the help of a 8 input Omega network. Explain routing from P4 to P7. **15**

(b) Write notes on cross bar network used in multiprocessor interconnection network. **5**

OR

13. Explain the following

(a) Full map directory based protocol. **10**

(b) Snoopy bus protocol. **10**