Reg. No. : .....

Name : .....

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F – 2950

Eighth Semester B.Tech. Degree Examination, December 2018
(2013 Scheme)
13.802 : COMPUTER SYSTEM ARCHITECTURE (R)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. Distinguish between multiprocessor and multicomputer based on their structures, resource sharing and inter-processor communications.

2. Compare and contrast temporal locality, spatial locality and sequential locality.

3. Characterize the architectural operations of SIMD and MIMD computers.

4. What is dataflow in Hybrid architecture ?

5. What is a hot-spot problem in interconnection network ? How is it handled ?

PART– B

Answer **any one** question from **each** Module. **Each** question carries **20** marks.

MODULE – 1

6. a) With proper block diagram describe the SIMD array processors and also explain how vector operations are efficiently handled by vector computer. **10**

   b) Describe how the three shared memory multiprocessor models differs in accessing the shared / distributed memory and peripheral resources. **10**

P.T.O.

7. a) The execution times (in seconds) of four program on three computers are given below :

Program	Execution time (in seconds)		
	Computer A	Computer B	Computer C
Program 1	1	10	20
Program 2	1000	100	20
Program 3	500	1000	50
Program 4	100	800	100

Assume that 100,000,000 instructions were executed in each of the four programs. Calculate the MIPS rating of each program on each of these three machines. Based on these rating, can you draw a clear conclusion regarding the relative performance of the three computers ? Give reasons if you find a way to rank them statistically. **10**

b) Prove that the best parallel algorithm written for an n-processor EREWPRAM model can be no more than *O(log n)* times slower than any algorithm for a CRCW model of PRAM having the same number of processors. **10**

MODULE – 2

8. Draw and explain the block diagram of a typical superscalar RISC processor architecture consisting of an integer unit and a floating-point unit. **20**

9. a) Explain in detail about various interleaved memory organization in multiprocessor system. **10**

b) Illustrate the working principle of busplane bus systems in detail. **10**

MODULE – 3

10. a) Suppose we want to design a pipelined adder (32bit, 8 stages) with basic ripple carry adders. Suppose a full adder delay is 1ns and clock skew is 10% setup time is 0.1s. What kind of pipelining is suitable for this scenario ? Justify your answer. **10**

b) State how linear vs. non linear pipelining got differentiated in their design perception. **10**

11. With proper example explain the instruction pipeline design and arithmetic pipeline design got implemented in the processor. **20**

MODULE – 4

12 . With appropriate example explain the various instruction issue and completion policies with and without instruction look ahead in a super scalar processor. **20**

13. a) Describe how the synchronization of four independent processes on four processors is implemented using Wired Barrier synchronization . **10**

b) Draw and explain the structure of mesh connected router with four pairs of I/O channels connected to neighboring routers. **10**