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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, March 2019
(2013 Scheme)
13.306 – DIGITAL ELECTRONICS (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **2** marks.

1. Given that $16_{10} = 100_B$ find the value of B.
2. Convert the following to max term.
   a) A(B + C′) b) A(A′ + B)(C′)
3. Draw the block diagram of sequential circuit and explain.
4. What are the applications of shift register ?
5. What is a twisted ring counter ?
6. Draw the logic diagram of a mealy model.
7. Compare mealy and moore machine.
8. Define the following terms with relation to digital IC.
   a) propagation delay b) fan out
9. Draw the basic write cycle timing diagram for SRAM.
10. Simplify the boolean expression A′BC + AB′C′ + A′B′C′ + AB′C + ABC.

PART – B

Answer **any one full** question from **each** Module. **Each full** question carries **20** marks.

Module – I

11. a) Obtain the minimal expression for F = Σm (1, 2, 3, 4, 5, 6, 7, 8, 9, 12, 13, 15) using tabular method. **15**

    b) Realize a full substractor using a 3-line to 8-line decoder. **5**

P.T.O.

12. a) Implement the following logic function using an 8 : 1 MUX.
F(A, B, C, D) = A′B + CD′ + AC′. **5**

b) Realize the switching function F(A, B, C) = Σm (2, 4, 5, 6) by a hazard free logic gate network. **5**

c) Simplify the Boolean expression using k map F = A′ + AB + ABD′ + AB′D′ + C and implement using NAND gate only. **10**

Module – II

13. a) Design and implement a synchronous 3bit up-down counter using JK flipflop. **15**

b) Calculate the frequency and dutycycle of the 555 astable multivibrator output for C = 0.01 μF, R_a = 10 kΩ, R_b = 50 kΩ. **5**

14. a) With neat logic diagram, explain race around condition in flipflops. How is it eliminated ? **8**

b) Design and implement a mod-10 asynchronous counter using T flipflop. **12**

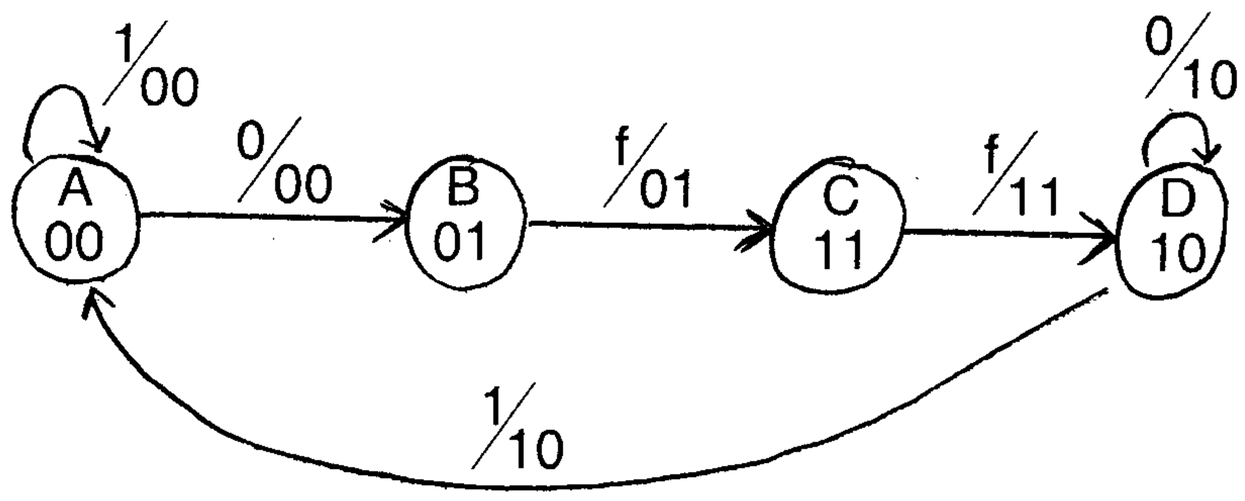
Module – III

15. a) A clocked sequential circuit with single input X and single output Z produces an output Z = 1 whenever the input X completes the sequence 1011 and overlapping is allowed

i) Obtain state diagram

ii) Obtain it's state transition table and design the circuit with D flipflops. **10**

b) Design a circuit that will function as prescribed by the state diagram as shown in fig. Using SR flipflop for implementation. **10**



16. a) Draw the state diagram and state table for a 3-bit odd parity generator. Use J-K flipflops for implementation. **15**

    b) Write the main steps involved in synthesis of synchronous sequential circuits. **5**

Module – IV

17. a) Show how an 8*1 PROM can be programmed to implement the logic function F = A′BC′ + A′BC + AB′C + ABC. **8**

    b) Compare the architecture of PAL and PROM. **6**

    c) What are the advantages and disadvantages of totem-pole configuration ? **6**

18. a) Write the VHDL code for a J-K flipflop with behavioral model. **10**

    b) With the help of a neat diagram explain static and dynamic RAM. **6**

    c) Implement the boolean function with PLA ; F_1 (A, B, C) = Σm (0, 1, 2, 4). **4**