

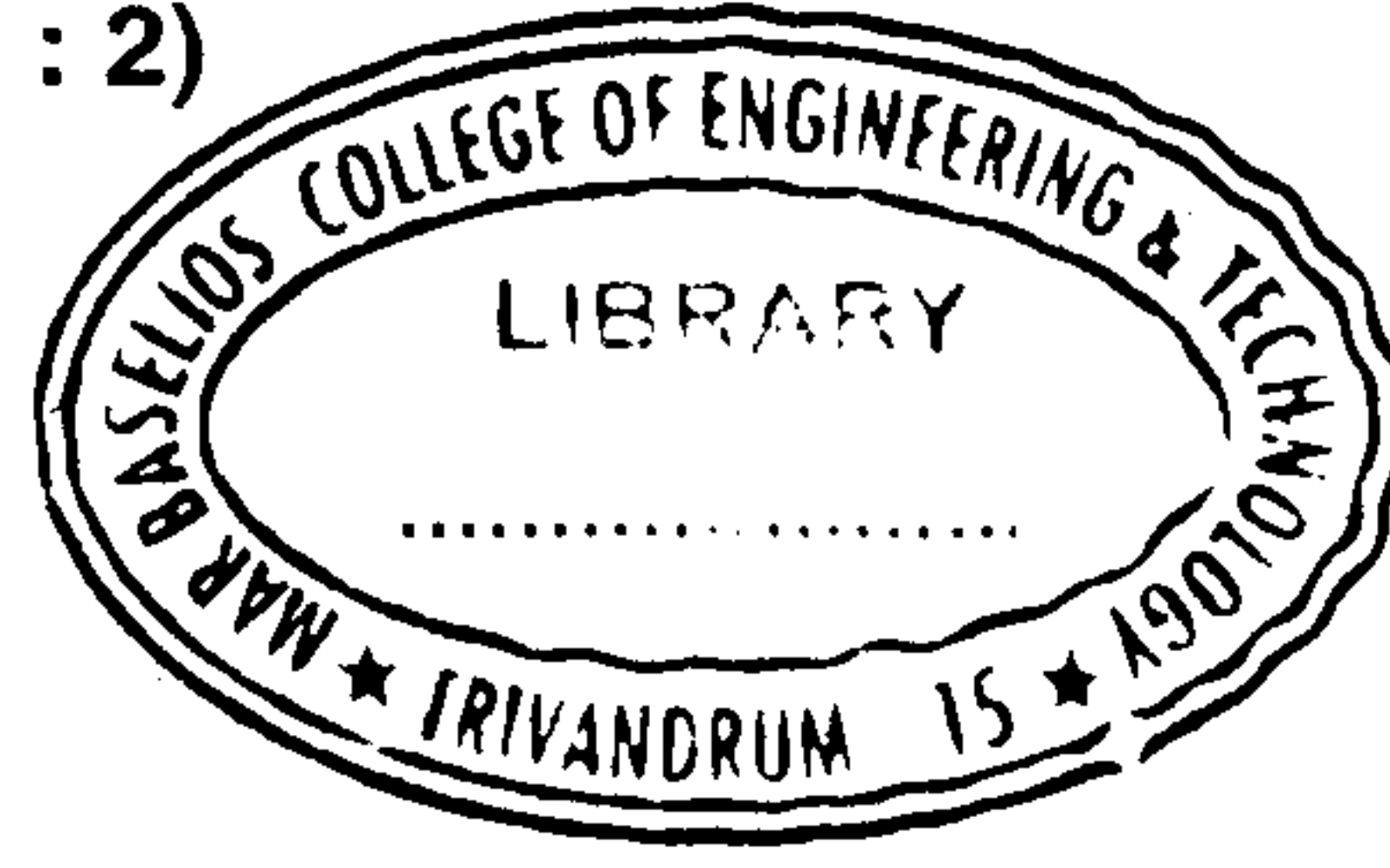


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F – 2212

Reg. No. :

Name :



**Third Semester B.Tech. Degree Examination, December 2018
(2008 Scheme)
08.306 : DIGITAL ELECTRONICS (T)**

Time : 3 Hours

Max. Marks : 100

PART – A

Answer **all** questions in Part **A**. **Each** question carries **4** marks.

1. State and prove DeMorgan's theorem.
2. Obtain the canonical sum of product form of the function $Y = A + BC$.
3. Write the VHDL code for a Half adder.
4. Differentiate static RAM from that of a dynamic RAM.
5. Show that a positive logic NAND gate is negative logic NOR.
6. Construct a JK flip flop using D and T flip flops.
7. What is a shift register ? Draw the universal shift register.
8. Differentiate Moore model from that of a Mealy model.
9. Draw the basic structure of an asynchronous sequential circuit.
10. Define static 0 and static 1 hazard. **(10×4=40 Marks)**

P.T.O.



PART – B

Answer **any 2** questions from **each** Module. **Each** question carries **10** marks.

Module – I

11. Reduce the following Boolean function using Quine-Mccluskey method
 $F(A, B, C, D) = \sum m (0, 1, 2, 3, 4, 6, 8, 10, 12, 14)$ 10
12. Explain how you will build a 64 input MUX using nine 8 input MUXs. 10
13. Write the VHDL code for a Full Adder. 10

Module – II

14. Draw and explain the circuit of two input CMOS NAND gate. 10
15. Elucidate how the flip flop timing specifications are important from its design point of view. 10
16. Using JK type design, design a synchronous counter for
 $0 \rightarrow 7 \rightarrow 5 \rightarrow 6 \rightarrow 1 \rightarrow 2 \rightarrow 0 \dots$ 10

Module – III

17. Design a sequence detector to detect the sequence 1101 with JK flip flops. 10
18. Explain how essential hazards and static hazards are eliminated. 10
19. Draw the logic diagram of the product of sums expression $Y = (X_1 + \bar{X}_2)(X_2 + X_3)$.
 Show that there is a static 0 hazard when X_1 and X_3 are equal to 0 and X_2 goes from 0 to 1. Find a way to remove the hazard by adding one more OR gate. 10

