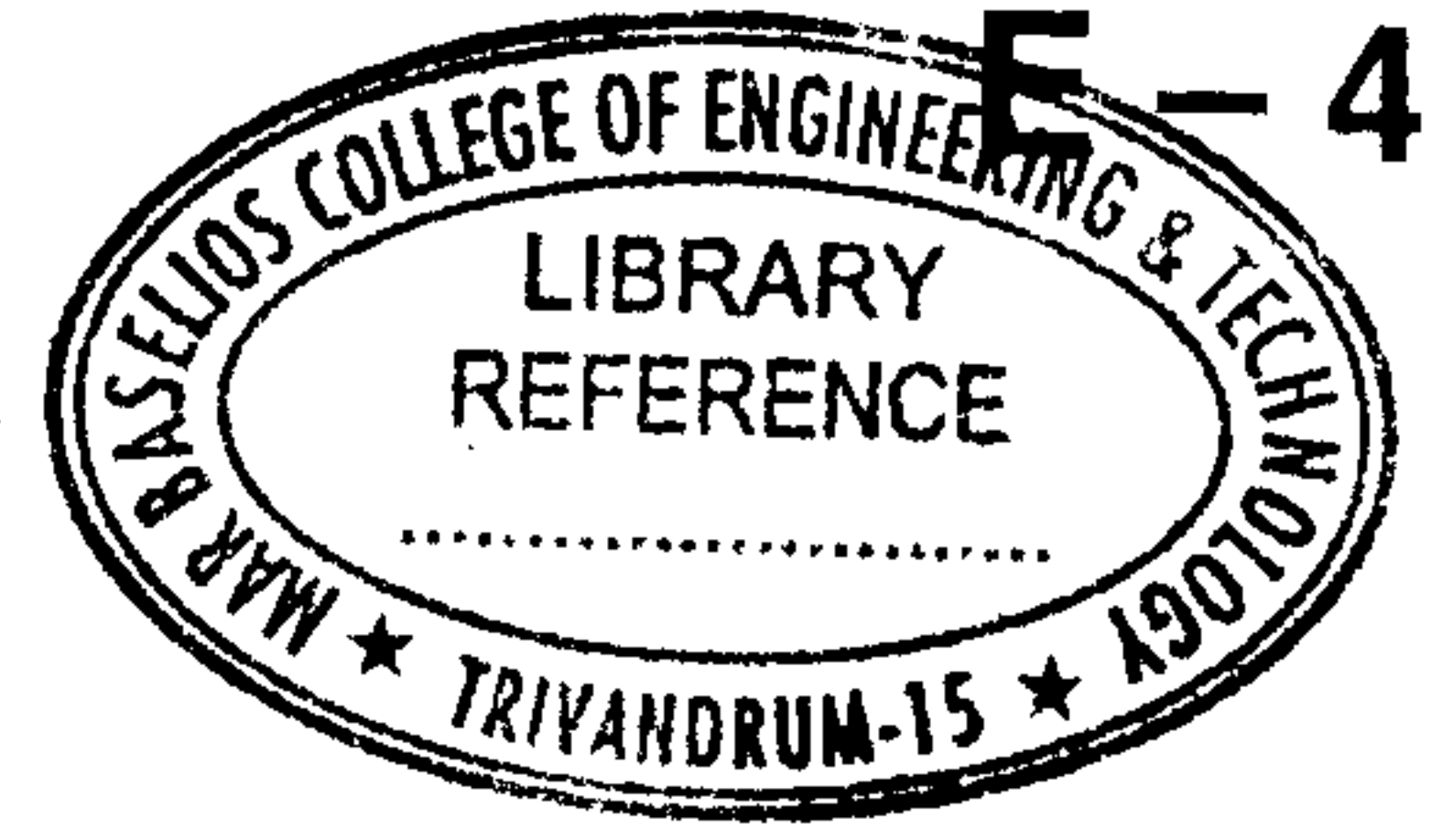




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Reg. No. :

Name :

**Fourth Semester B.Tech. Degree Examination, August 2018
(2013 Scheme)**

13.402 : COMPUTER ORGANIZATION AND DESIGN (FR)

Time : 3 Hours

Max. Marks : 100

PART – A

Answer **all** questions, **each** question carries **4** marks.

1. a) Write functions of the following registers (i) Program counter (ii) Stack pointer (iii) Instruction register (iv) Link register.
b) Using 2's complement arithmetic perform the following operations
(i) $(-6) + (-2)$ (ii) $(8) - (3)$.

2. Draw and explain the block diagram of a 4 bit ALU.

3. a) Two control functions at time T_2 are given as : $Q_1 T_2 : A \leftarrow A + B, E \leftarrow C_{out}$,
 $T_2 : P \leftarrow P + 1$. What are the conditions to execute the above statements ?

b) Using a 4 bit parallel adder with input A, B and C in and output as c_{out} and one selection input so, design arithmetic circuit as follows

S_0	Function
0	$A + B$
1	$B + 1$

4. a) Explain how the read and write operations are performed on the static RAM cell.
b) A block set associative cache consists of a total of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks, each consisting of 128 words. How many bits are there in main memory address ? How many bits are there in each of tag, set and word fields ?
5. Write the sequence of actions needed to fetch and execute the instruction load $R_5, X(R_7)$.

P.T.O.



PART - B

Answer **one full** question from **each** Module, **each full** question carries **20** marks.

Module - I

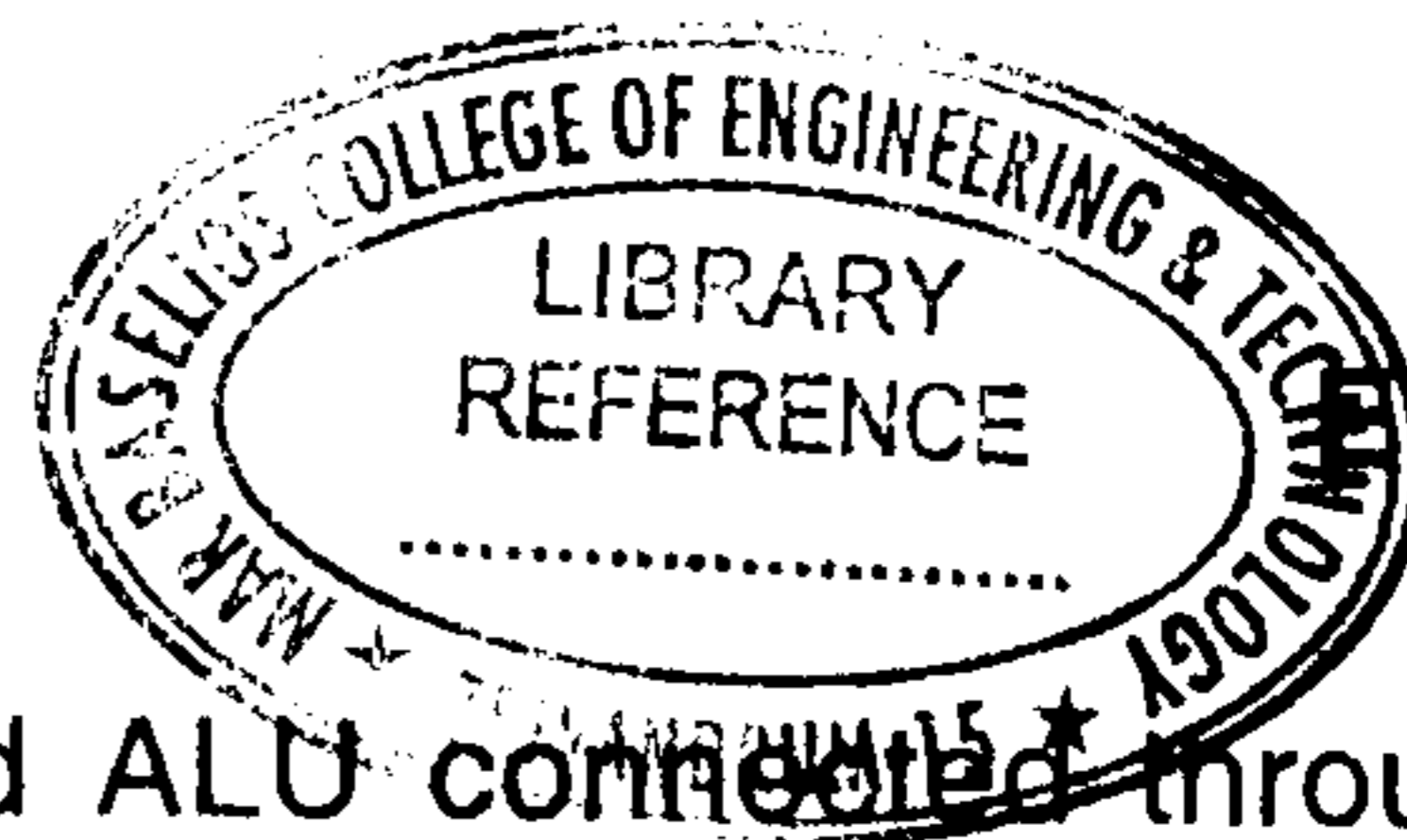
6. a) Explain the concept of indirect addressing mode by making use of the same in a sample program.
- b) What is byte addressable memory? With a neat diagram explain Big-Endian and Little-Endian assignment.
- c) Identify type of addressing modes for the given example.
 $EA = [R_i] + [R_j]$
 $EA = LOC.$
7. a) Briefly account on the following program controlled instructions with example for each
- Unconditional branch instruction
 - Conditional branch instruction
 - Subroutine call instruction
- b) Explain tasks performed by control unit.
- c) Explain following numbers in single and double precision IEEE floating point standard (i) 15.75 (ii) 25.25.

Module - II

8. a) Design an arithmetic circuit with two selection variables S_1 and S_0 that generates the following operations. Draw the logic diagram of one typical stage.

S_1	S_0	$C_{in} = 0$	$C_{in} = 1$
0	0	$F = A + B$	$F = A + B + 1$
0	1	$F = A$	$F = A + 1$
1	0	$F = \bar{B}$	$F = \bar{B} + 1$
1	1	$F = A + \bar{B}$	$F = A + \bar{B} + 1$

- b) Draw the data path of five stage organization with multiplexers and inter stage registers. Explain each stage of this organization.



9. a) Draw the diagram of processor registers and ALU connected through common bus.
- b) Design an adder/subtraction circuit with one selection variable S and two inputs A and B . When $S = 0$ the circuit performs $A + B$. $S = 1$ the circuit performs $A - B$ by taking the 2's complement of B .

Module – III

10. Explain with a figure, each functional unit of a Microprogram control for processor unit. How is it designed ?
11. Explain the design and organization of hardwired control Unit CPU.

Module – IV

12. a) Explain the 4 approaches of how multiple device initiating interrupts are handled by the processor with required diagram.
- b) Explain set associative mapping with example.
13. a) Explain the output interface circuit of the parallel part with diagram.
- b) A byte addressable computer has a small data cache capable of holding 8 32 bit words. Each cache block consists of one 32 bit word. When a given program is executed. The processor reads data from the following sequence of hex addresses : 200, 204, 208, 20C, 2F4, 200, 204, 218, 21C, 24C, 2F4. This pattern is repeated 4 times :
 - i) Show contents of cache at the end of each pass, through the above loop if a direct mapped cache is used. Compute hit rate. Assume cache is initially empty.
 - ii) Repeat this for 4-way set associative cache.