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Reg. No. : .....

Name : .....

Fourth Semester B.Tech. Degree Examination, September 2018
(2008 Scheme)
08.403 : COMPUTER HARDWARE DESIGN (R)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** carries **4** marks.

1. Draw the flowchart for Booth's algorithm.

2. What is an array multiplier ? Give the design for 2×3 array multiplier.

3. What is a normalised floating point number ? Give examples.

4. Give the hardware implementation for the statement $x'T_1$:A ←B.

5. Draw and explain a bus system with 4 registers.

6. Explain with the help of a diagram how a processor unit can be organised with a 2 port memory.

7. Explain the design of status register.

8. Describe the one flip flop per state method of control organisation.

9. Differentiate between horizontal and vertical microinstructions.

10. Draw and explain a micro programmed CPU organisation.

P.T.O.

PART – B

Answer **one** question from **each** Module.

Module – I

11. a) Explain the algorithm for addition and subtraction of two signed binary numbers. **12**

    b) Give the algorithm for BCD multiplication. **8**

OR

12. Draw and explain the flowchart for addition and subtraction of two floating point numbers. **20**

Module – II

13. a) Explain the different methods of processor organisation. **12**

    b) Explain arithmetic, logic and shift micro operations with examples. **8**

OR

14. a) Give the design of a 4 bit shifter. **8**

    b) Explain the design of accumulator. **12**

Module – III

15. Explain the design of micro program sequencer with the help of a diagram. **20**

OR

16. a) What are the different methods of control organisation ? **10**

    b) Write notes on nano memory and nano instructions. **10**