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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, May 2018

(2013 Scheme)

13.306 : DIGITAL ELECTRONICS (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **2** marks.

1. Write the 1's and 2's complement form of the decimal number –51.
2. Draw the logic diagram for the Boolean expression F = AB' + A'B.
3. Write the BCD and excess –3 code for the decimal number 59.
4. Distinguish between synchronous and asynchronous counter.
5. Write the truth table and characteristic equation of a SR flip-flop.
6. Mention the use of shift registers.
7. Write the state table for a D flip flop.
8. Distinguish between Moore and Mealy machine.
9. Define fan-in with reference to logic families.
10. Distinguish between ROM and PROM.

PART – B

Answer **any one** question from **each** Module. **Each full** question carries **20** marks.

Module – I

11.a) Minimize the function f = $\sum$ (0, 1, 2, 3, 4, 6, 8, 9, 10, 11) using K-map and implement using NOR gates. **10**

b) Explain the working of BCD to seven segment decoder. Draw the logic diagram and function table. **10**

OR

12. a) Explain the design and logic implementation of a look ahead carry adder. **10**

    b) Explain the design and implementation of a comparator to check the equality condition. **10**

Module – II

13. a) Explain the logic diagram, the different states in the working of a edge triggered D latch. **10**

    b) Describe with circuit diagram, working of an monostable multivibrator using 555IC. **10**

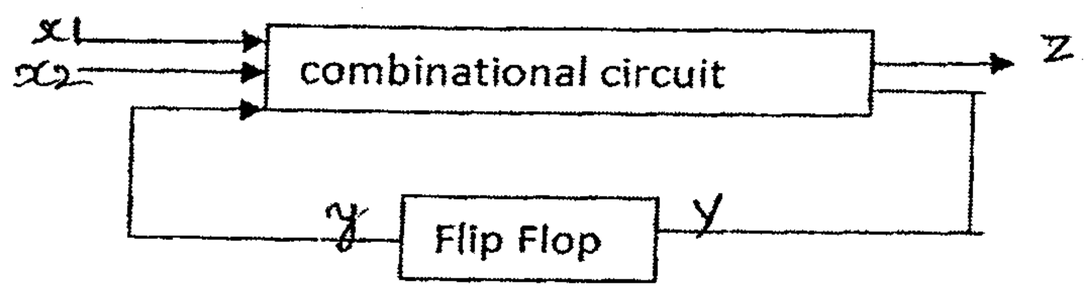
OR

14. a) Explain with diagram, the working of a 4 bit serial in serial out shift register. **10**

    b) Draw the diagram of a 3 bit ripple asynchronous counter using JK flip flop. Explain its operation using timing diagram. **10**

Module – III

15. a) Consider a serial binary adder with two binary inputs X_1 and X_2 to be added and one output terminal Z which represents the sum. The addition is to performed serially as shown below.



Draw the state diagram, state table, excitation table and transition table of the serial adder. Obtain the logic diagram of the circuit. **10**

    b) Explain the Moore model with example logic circuit and state equations. **10**

OR

16. a) Design a sequential circuit with four flipflops A, B, C and D. The next state of B, C and D are equal to the present states of A, B and C respectively. The next state of A is equal to the exclusive or of the present states of C and D. Write the state equations and draw the logic diagram using D • flipflops. **10**

b) Draw the state diagram, transition and output table for the sequential machine which has a single control input x and the clock and two outputs A and B. On consecutive rising edges of the clock, the code on A and B changes from 00 to 01 to 10 to 11 and repeats itself if x = 1. If at any time x = 0, it holds to the present state. **10**

Module – IV

17. a) Explain the organization of a memory cell and how reading and writing is accomplished in a memory cell. **10**

b) Write a VHDL code for implementing a 4 bit full adder. **10**

OR

18. a) Describe the working of Dynamic RAM memory cell and how DRAM refreshing is carried out. **10**

b) Explain the basic structure of PAL circuit and with an example explain how it can be used for implementing a function. **10**