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Reg. No. : .....

Name : .....

Eighth Semester B.Tech. Degree Examination, January 2018
(2013 Scheme)
13.802 : COMPUTER SYSTEM ARCHITECTURE (R)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **four** marks :

1. List the attributes used to measure the performance of a parallel computer.
2. Compare and contrast the characteristics of RISC and CISC architectures.
3. Distinguish between private caches and shared caches.
4. Define the following with respect to pipelining :
   Speedup, Efficiency and Throughput.
5. List the various Latency hiding techniques.

PART – B

Answer **any one full** question from **each** Module :

Module – 1

6. a) Analyze the data dependences among the following statements in a given program :

S_1 : Load R_1, 1024	/$R_1 \leftarrow$ 1024/
S_2 : Load R_2, M(10)	/$R_2 \leftarrow$ Memory(10)/
S_3 : Add R_1, R_2	/$R_1 \leftarrow (R_1) + (R_2)$/
S_4 : Store M (1024), R_1	/Memory(1024) $\leftarrow (R_1)$/
S_5 : Store M((R_2)), 1024	/Memory(64) $\leftarrow$ 1024/

P.T.O.

Where (R_i) means the content of register R_i and Memory (10) contains 64 initially.

i) Draw the dependence graph to show all the dependencies. **5**

ii) Are there any resource dependencies if only one copy of each functional unit is available in the CPU ? **5**

b) Describe in detail the three types of shared memory multiprocessor models. **10**

OR

7. a) Explain in detail the operational model of SIMD computers. **10**

b) Explain in detail the various dynamic interconnection architectures. **10**

Module – 2

8. Consider a two level memory hierarchy, M_1 and M_2. Denote the hit ratio of M_1 as 'h'. Let c_1 and c_2 be the costs per kilobyte, s_1 and s_2 the memory capacities and t_1 and t_2 the access times, respectively.

i) Under what conditions will the average cost of the entire memory system approach c_2 ? **4**

ii) What is the effective memory-access time t_a of this hierarchy ? **4**

iii) Let $r = t_2/t_1$ be the speed ratio of the two memories. Let $E = t_1/t_a$ be the access efficiency of the memory system. Explain E in terms of r and h. **4**

iv) Plot E against h for r = 5, 20 and 100, respectively. **4**

v) What is the required hit ratio 'h' to make $E > 0.95$ if $r = 100$? **4**

OR

9. a) Explain in detail the Direct mapping cache with an example. **10**

b) Describe in detail the Backplane bus system with a neat diagram. **10**

Module – 3

10. a) A non-pipelined process 'X' has a clock rate of 25 MHz and an average CPI (cycles per instructions) of 4. Processor Y, an improved version of 'X' is designed with a five-stage linear instruction pipeline. However, due to latch delay and clock skew effects, the clock rate of Y is only 20 MHz.

i) If a program containing 100 instructions is executed on both processors, what is the speedup of processor Y compared with that of processor X ? **5**

ii) Calculate the MIPS rate of each processor during the execution of this particular program. **5**

b) Explain in detail any of the Branch Handling Techniques. **10**

OR

11. Explain the various mechanisms used for instruction pipelining to smooth the pipeline flow. **20**

Module – 4

12. Explain in detail the various multiprocessor system interconnect architecture. **20**

OR

13. Describe in detail the various vector-access memory schemes. **20**