(Pages : 3) **D – 3550**

Reg. No. : .....

Name : .....

Eighth Semester B.Tech. Degree Examination, December 2017

(2008 Scheme)

08.802 : COMPUTER SYSTEM ARCHITECTURE (R)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. Write short notes on MFLOPS.
2. Brief on different variants of PRAM.
3. Compare and contrast perfect shuffle and inverse perfect shuffle.
4. Differentiate RISC and CISC processors.
5. Draw and explain a classic five stage pipeline for a RISC processor.
6. Describe the cache inconsistencies caused by process migration.
7. Write short notes on bus arbitration.
8. Consider a program of 15000 instructions executed by a linear pipeline processor with a clock rate of 25 MHz. The instruction pipeline has five stages and one instruction is issued per clock cycle. Calculate speed up ratio, efficiency and throughput of this pipelined processor.
9. Differentiate multi-computers and multiprocessors.
10. Describe wormhole routing. **(10×4=40 Marks)**

P.T.O.

PART – B

Answer **any one full** question from **each** Module.

Module – 1

11. a) Explain the various architectures of multiprocessor computers proposed by Michael Flynn with suitable diagrams. **15**

b) A 400-MHz processor was used to execute a benchmark program with the following instruction mix and clock cycle count :

Instruction type	Instruction count	Clock cycle count
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate and execution time for this program. **5**

OR

12. a) Explain the UMA, NUMA and COMA shared memory multiprocessor architectures with suitable diagrams. **8**

b) Explain the following static connection network topologies with necessary diagrams.

i) Ring and chordal ring. **3**

ii) Barrel shifter. **3**

iii) Fat tree. **3**

iv) Mesh and Torus. **3**

Module – 2

13. a) Explain the three principles of memory hierarchy for a system. **8**

b) Discuss virtual memory and virtual mapping with suitable diagrams. **12**

OR

14. a) Consider the following :

Main Memory Size : 32 MB

Cache Memory Size : 64 KB

Block Size : 4 B

Set Size : 4 Blocks

Discuss the associative and set associative mapping techniques with neat sketch by taking the above scenario as example. **10**

b) Explain the sequential, strict and weak consistency models of shared memory with suitable diagrams. **10**

Module – 3

15. a) Explain any three sources of cache data inconsistency and discuss the possible protocols to overcome the cache data inconsistency problem. **10**

b) Explain the crossbar switch design with suitable examples. **10**

OR

16. a) Explain the distributed and scalable coherent caches and their architectures with necessary diagrams. **10**

b) Describe in detail the multithreading and its associated principles. **10**