C – 5368

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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, October 2017
(2008 Scheme)
08.305 : ELECTRONIC CIRCUITS – I (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. Derive the expression for ripple factor of HWR.
2. Draw the response of a high pass RC circuit to step input and square wave input.
3. A 100 V peak square wave with an average value of 0 V and a period of 20 ms is to be negatively clamped at 25 V. Draw the circuit diagram, input and output waveforms.
4. Discuss the significance of TUF and ripple factor in a rectifier circuit.
5. A FWR uses a capacitor filter of 1000 μF and provides a dc load current of 500 mA at 2% ripple. Calculate a) dc output voltage and b) % regulation.
6. Comment on the combined impact of changes in I_{CB0}, V_{BE} and β on the Q point stability.
7. Draw the small signal model for an FET and explain.
8. Draw the block diagram of a regulated dc power supply.
9. What is cross over distortion ? Draw its transfer characteristics. How is it eliminated ?
10. Discuss the classification of Class A, B and AB amplifier. **(10×4=40 Marks)**

PART – B

Answer **any two** questions from **each** Module. **Each** question carries **10** marks.

Module – I

11. A bridge rectifier uses load resistor $R_b = 3K\Omega$. Each diode has idealized characteristics with slope resistance $R_f = 8\Omega$ and $R_r = \infty$. Cut-in voltage may be assumed to be zero. Input sinusoidal voltage in each half cycle has amplitude of 25 V and frequency 50 Hz. Calculate a) peak dc and rms values of load current b) dc output power c) rectifier efficiency and d) % regulation.

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12. Draw the circuit diagram of low pass RC circuit. Explain its working. Plot the response for any periodic input and obtain necessary design equation.

13. With circuit diagram, explain the working of BJT shunt regulator.

Module – II

14. Using low frequency model, derive expression for A_i, A_v, Z_i and Z_o of a CE amplifier.

15. For an FET circuit biased using source self-bias scheme, $V_{DD} = 24$ V, $R_D = 4.7\,K\Omega$, $R_G = 10\,M\Omega$ & $R_S = 820\ \Omega$. For the FET $g_{m0} = 2.5$ m and $I_{DSS} = 5$ mA. Calculate operating point.

16. With schematic, explain a fixed bias circuit. Derive expression for stability factor.

Module – III

17. Draw the circuit diagram of class B push pull power amplifier. Explain its working and derive the expression for efficiency.

18. Analyse the high frequency response of CE amplifier and derive the expression for voltage gain. Explain Miller capacitance.

19. A given transistor operating at $I_C = 8$ mA, $V_{CE} = 10$ V and room temperature (300 K) has the following low frequency parameters. $h_{ie} = 600\ \Omega$, $h_{oe} = 2\times10^{-4}\ \mu S$, $h_{fe} = 90$ and $h_{re} = 2\times10^{-4}$. At the same operating point $f_T = 40$ MHz and $C_c = 4$ pF. Calculate the values of hybrid π parameter.