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C – 5369

Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, October 2017
(2008 Scheme)
08.306 : DIGITAL ELECTRONICS (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions :

1. Classify the binary codes and convert the following :
   a) $(13.25)_D$ to BCD
   b) $(14.75)_D$ to Excess 3
   c) $(110101)_b$ to Grey
   d) $(1101101.01)_b$ to Hex

2. Represent the given function using AOI gates and realize the same using NAND only after simplification using Boolean algebra.

   $Y = (A + B)(\bar{A}\bar{C} + C)(\overline{\bar{B} + AC})$

3. Simplify the given function using K-map and mark the PI, EPI and Redundant Prime Implicants.

   $Y = \bar{A}CD + ABC + A\bar{C}D + \bar{A}B\bar{C}$

4. State and verify De-Morgan's theorem.

5. Distinguish between Mealy and Moore models of state machines.

6. Describe the basic structure of static and dynamic RAM cell.

7. Discuss the various methods for architectural declaration in VHDL and write the VHDL program for a 4 × 1 multiplexer.

P.T.O.

8. Define the following terms and write the values for TTL and CMOS logic families.
   a) Noise margin
   b) Propagation delay
   c) Fan-out
   d) Power consumption

9. What is race around problem ? Describe the methods for eliminating the same.

10. Distinguish between the re-triggerable and non re-triggerable monostable multivibrators with examples. **(10×4=40 Marks)**

PART – B

Answer **any two** questions from **each** Module.

Module – 1

11. Simplify the given Boolean function using tabulation method
    $F = \sum m(0, 1, 2, 8, 10, 11, 14, 15)$

12. Design a BCD to seven segment decoder for a common anode display and discuss the features of IC 7447.

13. a) Realize a four bit adder/subtraction circuit and explain the working with examples.
    b) Design and realize a decimal to BCD priority encoder.

Module – 2

14. a) Explain the working of SR flipflop with schematic diagram, truth table and characteristic equation.
    b) Realize a MOD-6 asynchronous counter and explain the operation with state and timing diagram.

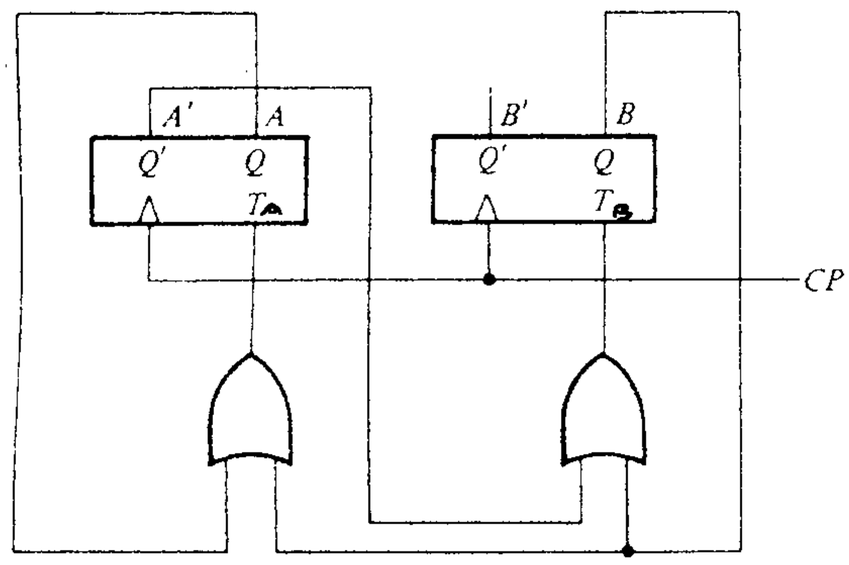
15. Design a synchronous counter for counting the sequence 1, 5, 3, 6, 2, 1 ... using T flip-flop.

16. a) Realize a universal shift register and explain the operation with control signals.
    b) Explain the working of NOR, NAND and NOT gates using CMOS with circuit diagram and truth tables.

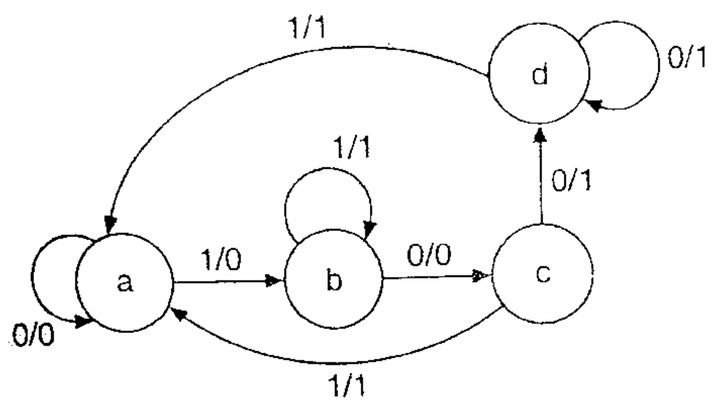
Module – 3

17. Design a Mealy type synchronous sequence detector using D flip-flop which produces an output "Z = 1" when a non-overlapping sequence "0101" is detected. Changes in the signal (x) are synchronous with negative going edge of the clock.

18. Derive the state table and state diagram of the given sequential circuit and identify the function of the circuit.



19. a) Obtain the reduced state-table and reduced state diagram for the given state diagram.



b) Describe the terms race, cycles and hazards associated with sequential circuits.