Reg. No. : .....

Name : .....

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C – 2643

First Semester M.Tech. Degree Examination, June 2017
(2013 Scheme)
Branch : Computer Science and Engineering
RCC 1005 : ADVANCED COMPUTER ARCHITECTURE

Time : 3 Hours

Max. Marks : 60

***Instruction** : Answer **2** questions from **each** Module.*

MODULE – I

1. a) Determine the number of clock cycles required to process a program with 200 instructions six segment pipeline. **3**

   b) Estimate the CPU time needed for executing 70 K program with a processor of speed 100 MIPS. **3**

   c) A processor speed 2GHz is used to execute a program with the following details :

Arithmetic instructions	40K	1(CPI)
Memory instructions	15K	2 (CPI)
Control instructions	5K	2 (CPI)
I/O instructions	10K	3 (CPI)

   Find the CPU time needed for the execution of the program. **4**

2. a) Derive an expression for overall speedup according to Amdahl' Law. **4**

   b) A processor architecture is modified such that it is 30 times faster on computation in web processing than the original processor. Original processor is busy with computations 40% of time and is waiting for I/O 60% of time. What is the overall speedup gained ? **3**

   c) Explain the concept of forwarding mechanism in pipelining. **3**

P.T.O.

3. a) Write the dependencies existing between the various instructions in the following code. **3**

```
DIV.D    F0, F2, F4
ADD.D    F6, F0, F8
S.D      F6, 0(R1)
SUB.D    F8, F10, F14
MUL.D    F14, F1, F10
```

b) Explain the concept of loop unrolling with an example. **4**

c) Write notes on different type of hazards. **3**

MODULE – 2

4. a) Explain dynamic scheduling using Tomasulo's approach with figure. **7**

b) Point out the differences between Tomasulo's approach and hardware based speculation. **3**

5. a) Explain about Branch-Target buffer and the steps involved in handling an instruction with a branch-targer buffer. **6**

b) Explain how strides can be used for handling multidimensional arrays in vector architecture. **4**

6. a) Explain the following terms in connection with vector architecture. **5**

i) convoy

ii) chaining

iii) chime

b) Show how the following code sequence lays out in convoys, assuming a single copy of each vector functional units. How many chimes this vector sequence will take ? **5**

```
LV        V1, Rx      ; load vector Rx
MULVS.D   V2, V1, F0  ; vector-scalar multiply
LV        V3, Ry
ADDVV.D   V4, V2, V3  ; add two vectors
SV        V4, Ry      ; store the sum
```

MODULE – 3

7. a) Explain about hierarchial bus system. **5**

   b) Explain about blocking and non-blocking networks. Write suitable examples for each. **5**

8. a) Draw an 8 × 8 Omega network built with 2 × 2 switches for the permutation (0, 7, 6, 4, 2) (1, 3) (5). Explain the routing of a message from input 110 to output 100. **7**

   b) Show how an 8 × 8 Omega network can be used to broadcast data from one source to all the destinations. **3**

9. a) What is cache coherence problem ? Explain the reasons which cause cache inconsistencies. **5**

   b) Explain the Snoopy bus protocols. **5**