(Pages : 2) **B – 2668**

Reg. No. : .....

Name : .....

Eighth Semester B.Tech. Degree Examination, December 2016
(2008 Scheme)
08.802 : COMPUTER SYSTEM ARCHITECTURE (R)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions : **(10×4=40 Marks)**

1. State the Flynn's classification of computer architectures and their features.

2. What are the new challenges that demand parallel processing ?

3. Illustrate how the system attributes affect the performance factors used for measuring the efficiency of the system.

4. What are the issues to be addressed when a computer is scaled up to perform massively parallel processing operations ?

5. Compare the features of superscalar and vector processors.

6. What are the various locality properties of memory reference patterns ?

7. How is a co-processor different from a processor ?

8. List the cache events and actions.

9. What is latency hiding ? What are the latency hiding techniques ?

10. What are the scalability issues of shared virtual memory systems ?

P.T.O.

PART – B

Answer **one** question from **each** Module. **Each** question carries **20** marks.

(3×20=60 Marks)

Module – I

11. i) Characterize the architectural operations of SIMD and MIMD computers. **8**

ii) Distinguish between the multiprocessor and multicomputer systems. Explain the features of NUMA and COMA computers. **12**

OR

12. i) What are the conditions of parallelism ? Compare and contrast hardware and software parallelisms with an example problem. **12**

ii) Discuss briefly about various system inter connect architectures. **8**

Module – II

13. i) Explain how pipelining is implemented in superscalar processors. **10**

ii) Explain the architecture of very long instruction word processor and its pipeline operations with a neat diagram. **10**

OR

14. i) Discuss about the performance metrics used for measuring the pipeline efficiency. **8**

ii) Explain the Tomasolu's algorithm for dynamic instruction scheduling and show how it handles the hardware dependency of pipeline execution. **12**

Module – III

15. i) Discuss briefly about the multiport memory organization of multiprocessor systems. **8**

ii) What are the causes of cache inconsistency ? Explain the mechanisms used for handling cache inconsistencies. **12**

OR

16. i) With a neat diagram explain the architecture of intel paragon multicomputer. **10**

ii) Discuss briefly about full scale vector supercomputers. **10**