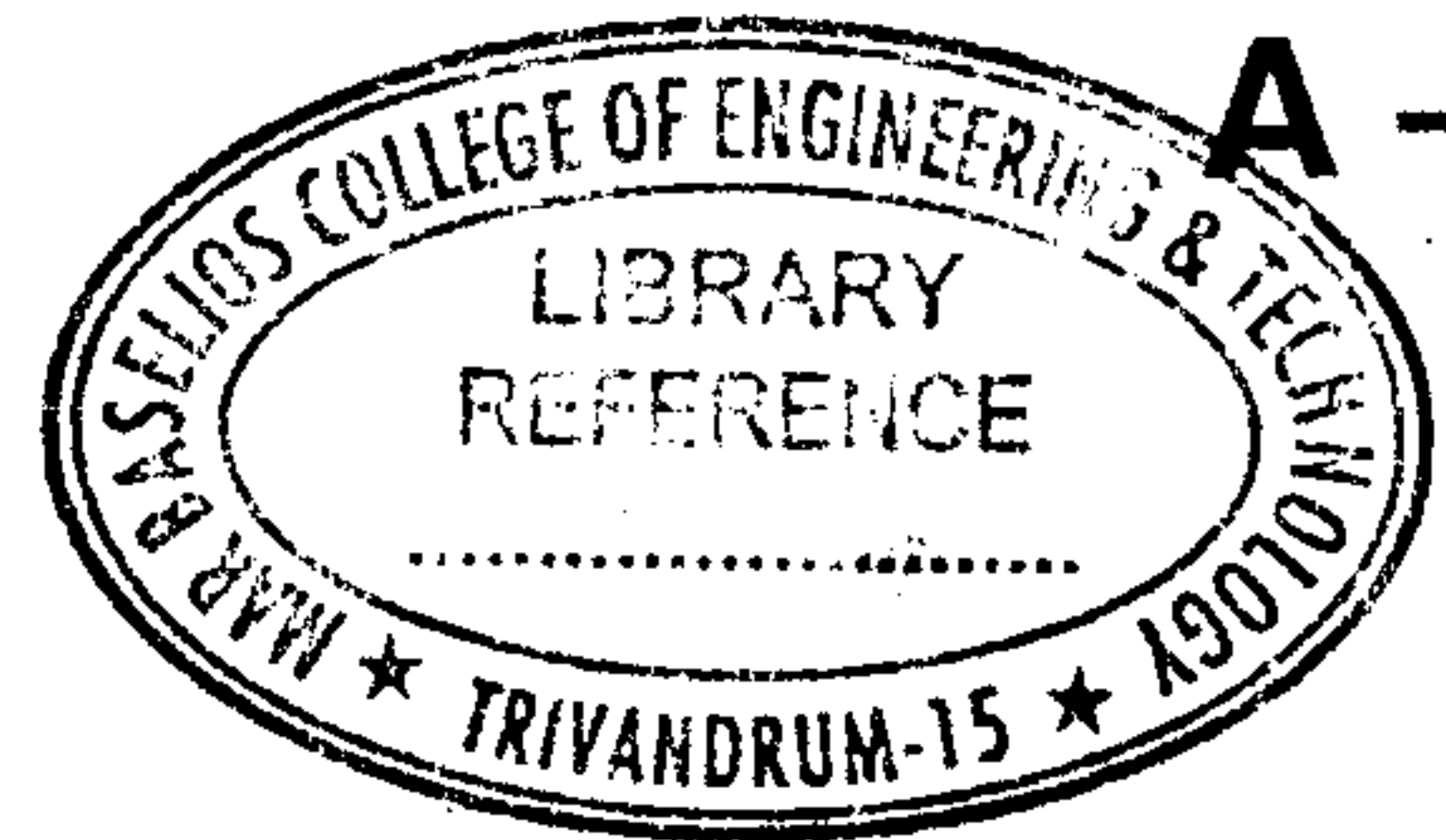




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A – 6589

Reg. No. :

Name :

**Third Semester B.Tech. Degree Examination, October 2016
(2013 Scheme)
13.306 : DIGITAL ELECTRONICS (T)**

Time : 3 Hours

Max. Marks : 100

PART – A

Answer **all** questions :

(10×2=20 Marks)

1. Express – 45 in 8 bit 2's complement form.
2. Find a solution to the following expression by applying DeMorgan's theorem.
 $((AB)' + A' + AB)'$.
3. List the three important applications of multiplexers.
4. Show the construction of T flip flop using JK flip flop.
5. What is universal shift register ?
6. Draw the circuit of free running multivibrator using Schmitt trigger.
7. Give out the state diagram of serial binary adder.
8. What information does the excitation table give ?
9. Define the propagation delay and fanout of a digital IC.
10. What are the alternate names given for Electrically Erasable PROM ?

P.T.O.



PART – B

Answer **any one** question from **each** Module.

Module – I

11. a) Convert the following Gray code into Binary : 101101. 2
- b) Prove that $(A + B)(A' + C)(B + C) = (A + B)(A' + C)$ using Consensus theorem. 4
- c) Obtain the minimal expression using the tabular method :
 $\Sigma m(0, 1, 3, 4, 5, 7, 10, 13, 14, 15)$. 8
- d) Which is the arithmetic circuit that adds two bits and an input carry and outputs a sum bit with a carry ? Give out its logic diagram with truth table. 6
12. a) How does the BCD to Seven segment decoder operate ? Give out the expression for driving any one of the segment. 5
- b) Use a multiplexer to implement the logic function : $F = A.(EXOR).B.(EXOR).C$. 7
- c) Show a typical key board encoder consisting of a diode matrix used to encode the 10 decimal digits and discuss its operation. 8

Module – II

13. a) Define and comment on the following operating characteristics of flip flops. 8
- i) Power dissipation
 - ii) Clock skew and time race
 - iii) Potential timing problem
 - iv) Set up and hold time
- b) Obtain the excitation table and K map reduction for the implementation of BCD counter using JK flip flop. 12
14. a) Design and implement a mod – 6 Asynchronous counter using T flip flops. 10
- b) Construct a one-shot circuit using NOR gate and an inverter. Elaborate its working principle with the time delay expression. 10



Module – III

- 15. a) A long sequence of pulses enters a 2 input 2 output synchronous sequential circuit which is required to produce an output $Z = 1$, whenever the sequence 1101 occurs. Overlapping sequences are accepted. Design the circuit. **15**
- b) Write the main steps involved in the synthesis of synchronous sequential circuits. **5**
- 16. a) Design a 3 bit up/down counter which counts up when the control signal $M = 1$ and counts down when $M = 0$. **15**
- b) How do asynchronous sequential circuits differ from synchronous sequential circuits ? List various memory elements used in sequential machines. **5**

Module – IV

- 17. a) With the help of neat circuit diagram, explain the working of two input TTL Nand gate. **10**
- b) Show the construction of PAL to implement the function $f = AB'C + A'BC$. **10**
- 18. a) What is DRAM refreshing ? Why is it needed ? **5**
- b) How does a PROM differ from an UROM ? Can it be erased and reprogrammed ? **4**
- c) Tabulate the differences of sequential access memory and random access memory. **5**
- d) Compare the architecture of PAL and PROM. **6**

