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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, September 2016
(2008 Scheme)
08.306 : DIGITAL ELECTRONICS (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. Prove that $\bar{a}\bar{b} + b\bar{c} + ac + \bar{b}c = \bar{a}\bar{b} + ac + b\bar{c}$.
2. Explain how a demultiplexer can be obtained from a decoder.
3. Differentiate ripple carry and look ahead carry adders.
4. Obtain the characteristic equation of a D-flipflop.
5. What is meant by hazards in logic circuits ? What are its causes ?
6. What is tristate TTL ? Explain.
7. Define a synchronous sequential machine.
8. Differentiate retriggerable and non-retriggerable monostable multivibrators. Give examples for each.
9. Define a Moore machine and draw its general model.
10. Convert a given D-flip flop into T-flip flop. **(10×4=40 Marks)**

PART – B

Answer **any two** questions from **each** module. **Each** question carries **10** marks.

Module – I

11. Using K-map, determine all prime implicants, essential prime implicants and the minimal expression. Realise the function using gates.
    $F(a, b, c, d) = \Sigma(0, 1, 2, 3, 4, 6, 7, 8, 9, 11, 15)$

P.T.O.

12. a) Compare PROM, EPROM and EEPROM.

    b) Implement F(a, b, c, d) = Σm(0, 1, 2, 3, 12, 14, 15) using an appropriate multiplexer.

13. a) Explain the working of a decoder module.

    b) Write a VHDL program for a full adder.

Module – II

14. a) Explain the working of a 2-input TTL NAND gate.

    b) Explain how the propagation delay is reduced in Schottky TTL gate.

15. Design a circuit that acts as a mode 4 counter when the control input is 'zero' and as a mode-6 counter when the control input is 'one'.

16. Draw the schematic of a universal shift register. Explain its working. Discuss its use as a parallel-to-serial converter.

Module – III

17. a) Explain in brief the elimination of hazards in combinational circuits of types :

    i) static

    ii) dynamic and

    iii) essential.

    b) Implement a hazard free circuit for the following :

    $f(A\ B\ C\ D) = \overline{A}B\overline{C} + \overline{A}\,\overline{B}D + C\overline{D} + AC$

18. A system with one input x and one output z such that z = 1 iff x has been '1' for atleast 3 consecutive clock time. Implement using D flipflop as a Moore machine.

19. An asynchronous network has two inputs and one output. The input sequence x_1x_2 = 00, 01, 11 causes the output to become 1. The next input change then causes the output to return to 'zero'. No other input sequence will produce a 'one' output. Develop the flow table. **(6×10=60 Marks)**