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Reg. No. : .....

Name : .....

Eighth Semester B.Tech. Degree Examination, November 2015
(2008 Scheme)
08.802 : COMPUTER SYSTEM ARCHITECTURE (R)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. List out the metrics affecting the scalability of a computer system for a given application.

2. Which PRAM variant can best model SIMD machines and how ?

3. Distinguish between register-to-register and memory-to-memory architecture for building conventional multivector supercomputers.

4. Explain how instruction set and memory hierarchy affect the CPU performance in terms of clock rate, program length and effective CPI.

5. Distinguish between multiprocessors and multicomputers based on their structures, resource sharing and interprocessor communications.

6. What is the significance of Bernstein's condition to detect parallelism ?

7. Compare temporal locality and spatial locality of references.

8. Distinguish between static and dynamic interconnection network.

9. Describe bus arbitration in multiprocessor system.

10. Describe the cache inconsistencies caused by process migration. **(10×4=40 Marks)**

P.T.O.

PART – B

Answer **one full** question from **each** Module. **Each** question carries **20** marks.

MODULE – I

11. a) Analyse the dependencies among the following statements in a given program. Show the dependence graphs among the statements with justification.

i) DO 10 I = 1, N
A(I + 1) = B(I – 1) + C(I)
B(I) = A(I) * K
C(I) = B(I) – 1
10 CONTINUE

ii)

S1 : Load R1, M(100)	/R1 ← Memory(100)/
S2 : Move R2, R1	/R2 ← (R1)/
S3 : Inc R1	/R1 ← (R1) + 1/
S4 : Add R2, R1	/R2 ← (R2) + (R1)/
S5 : Store M(100), R1	/Memory(100) ← (R1)/

Where (Ri) means the content of register Ri.

i) Draw dependence graph to show all the dependencies with justification.

ii) Are there any resource dependencies if only one copy of each functional unit is available in the CPU ? **12**

b) List the basic differences between UMA, NUMA and COMA models. **8**

OR

12. a) A workstation uses a 15 MHz processor with a claimed 10-MIPS rating to execute a given program mix. Assume one cycle delay for each memory access.

i) What is the effective CPI of this computer ?

ii) Suppose the processor is being upgraded with a 30 MHz clock. However the speed of the memory subsystem remains unchanged and consequently two clock cycles are needed per memory access. If 30% of the instructions require one memory access and another 5% require two memory accesses per instruction, what is the performance of the upgraded processor with a compatible instruction set and equal instruction counts in the given program mix ? **12**

b) Explain in detail about various interleaved memory organization in multiprocessor system. **8**

MODULE – II

13. Consider the five-stage pipelined processor specified by the following reservation table :

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

a) List the set of forbidden latencies and collision vector.

b) Draw state transition diagram showing all possible initial sequences (cycle) without causing a collision in the pipeline.

c) List all the simple cycles from the state diagram.

d) Identify the greedy cycles among the simple cycles.

e) What is the Minimum Average Latency (MAL) of this pipeline ?

f) What is the minimum allowed constant cycle in using this pipeline ?

g) What will be the maximum throughput of this pipeline ?

h) What will be the throughput if the minimum constant cycle is used ? **20**

OR

14. a) Explain the concept of arithmetic pipeline design. **10**

b) Discuss the various instruction issue and completion policies with and without instruction look ahead in a superscalar processor. **10**

MODULE – III

15. a) Explain any two cache coherence protocol. **10**

b) Explain the Intel Paragon System architecture with a neat schematic sketch. **10**

OR

16. a) Describe how multiport memories are used in multistage networks. Explain blocking and non-blocking network with the help of Omega network. **10**

b) Describe data flow and hybrid architecture. **10**

(3×20=60 Marks)