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Reg. No. : .....

Name : .....

First Semester M.Tech. Degree Examination, February 2015
(2013 Scheme)
Branch : Electrical and Electronics Engineering
Streams : Power Control and Drives, Industrial Instrumentation and Control
EIC 1002 : ADVANCED SIGNAL PROCESSING

Time : 3 Hours Max. Marks : 60

***Instructions** : 1) Answer **any two** questions from **each** Module.*
*2) **All** questions carry **equal** marks.*

Module – I

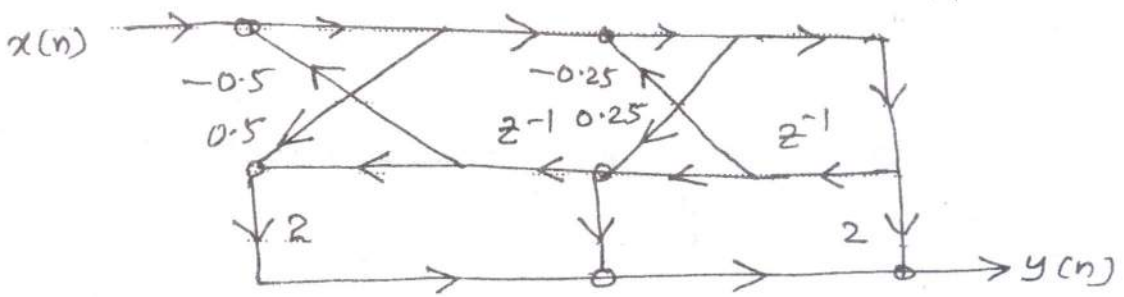
1. Find the 2-D Z-transform and region of convergence of

   a) $u_{++}(n_1, n_2)$

   b) $u_{+-}(n_1, n_2)$

2. g(n) and h(n) are two sequences of length 6. The 6-point DFTs are G (K) and H(K) respectively. Given g(n) = {4.1, 3.5, 1.4, 5, 3.3, 2.7}. G(K) and H(K) are related by the expression $H(K) = G((K-3))_6$. Determine h (n) without computing DFT or IDFT.

3. Find the system function of the following lattice filter



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Module – II

4. Design an FIR linear phase filter using Hamming window approximating the response $H(e^{jw}) = 1$, for $|\omega| \leq \pi/4$

$= 0$, for $\frac{\pi}{4} < |\omega| \leq \pi$

Assume filter length L = 13. Draw the filter structure in direct form.

5. Determine the variants of the round off noise at the output of the cascade realizations of the filter $H(z) = 1 + 2.88\, z^{-1} + 3.404\, z^{-2} + 1.74 z^{-3} + 0.4\, z^{-4}$.

6. A second order normalised lowpass Butterworth filter is $H(s) = \frac{1}{s^2 + \sqrt{2}s + 1}$.

Obtain the following filters using Bilinear transformation

a) digital low pass filter with cut-off frequency = 2 rad.

b) digital bandpass filter with cutoff frequencies 1 rad and 2 rad.

Module – III

7. Consider a speech system with the following specifications :

Speech input frequency range : 0-4 KHz,

ADC resolution = 16 bits, current sampling rate = 8 KHz.

a) Determine the oversampling rate if a 12-bit ADC chip is used to replace the speech system.

b) Draw the block diagram.

8. Consider a sampling conversion DSP system. Audio input sampled at 6 KHz. Audio output to be operated at 9 KHz. Draw the block diagram of the system giving relevant details for desiging.

9. Explain briefly the architecture of ADSP 2181 processor. Compare the architecture of a DSP processor with a general purpose processor. **(6×10 = 60 Marks)**