CS

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Reg. No. : .....

Name : .....

**Eighth Semester B.Tech. Degree Examination, October 2014**

**(2008 Scheme)**

**08.802 : COMPUTER SYSTEM ARCHITECTURE (R)**

Time: 3 Hours Max. Marks: 100

PART – A

**(Answer all questions)**

1. Which PRAM variant can best model SIMD machines and how ?
2. List out the metrics affecting the scalability of a computer system for a given application.
3. Distinguish between multiprocessors and multicomputers based on their structures, resource sharing and interprocessor communications.
4. Describe the memory level hierarchy.
5. Compare temporal locality, spatial locality and sequential locality.
6. Describe bus arbitration in multiprocessor system.
7. What is meant by memory interleaving ?
8. Characterize the architectural operations of SIMD and MIMD computers.
9. What is the use of crossbar network ?
10. Describe briefly about the Flynn's classification. **(10×4=40 Marks)**

P.T.O.

PART – B

**(Each question carries 20 marks)**

**Module – I**

11. a) A workstation uses a 15 MHz processor with a claimed 10-MIPS rating to execute a given program mix. Assume one cycle delay for each memory access.

    i) What is the effective CPI of this computer ?

    ii) Suppose the processor is being upgraded with a 30 MHz clock. However the speed of the memory subsystem remains unchanged, and consequently two clock cycles are needed per memory access. If 30% of the instructions require one memory access and another 5% require two memory accesses per instruction, what is the performance of the upgraded processor with a compatible instruction set and equal instruction counts in the given program mix ?

    b) List the difference between UMA, NUMA and COMA models.

OR

12. a) Distinguish between register-to-register and memory-to-memory architecture for building conventional multivector supercomputers.

    b) Analyze the data dependences among the following statements in a given program :

| | | |
|---|---|---|
| S1 : | Load R1, 1024 | /R1 $\leftarrow$ 1024/ |
| S2 : | Load R2, M(10) | /R2 $\leftarrow$ Memory(10)/$\tau$ |
| S3 : | Add R1, R2 | /R1 $\leftarrow$ (R1) + (R2)/ |
| S4 : | Store M(1024), R1 | /Memory (1024) $\leftarrow$ (R1)/ |
| S5 : | Store M((R2)), 1024 | /Memory(64) $\leftarrow$ 1024/ |

    Where (Ri) means the content of register Ri and Memory(10) contains 64 initially.

    i) Draw dependence graph to show all the dependences.

    ii) Are there any resource dependences if only one copy of each functional unit is available in the CPU ?

## Module – II

13. a) Consider the execution of a program of 15000 instructions by a linear pipeline processor with a clock rate of 25 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instruction and out-of-sequence executions are ignored.
    i) Calculate the speed up factor in using this pipeline to execute the program as compared with the use of an equivalent nonpipelined processor with an equal amount of flow-through delay.
    ii) What are the efficiency and throughput of this pipelined processor ?

    b) Explain in detail about various interleaved memory organization in multiprocessor system.

OR

14. Consider the three-stage pipelined processor specified by the following reservation table :

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| S1 | X | | | | | X | | X |
| S2 | | X | | X | | | | |
| S3 | | | X | | X | | X | |

i) List the set of forbidden latencies and collision vector.

ii) Draw state transition diagram showing all possible initial sequences (cycle) without causing a collision in the pipeline.

iii) List all the simple cycles from the state diagram.

iv) Identify the greedy cycles among the simple cycles.

v) What is the Minimum Averages Latency (MAL) of this pipeline ?

vi) What is the minimum allowed constant cycle in using this pipeline ?

vii) What will be the maximum throughput of this pipeline ?

viii) What will be the throughput if the minimum constant cycle is used ?

## Module – III

15. a) Explain any two cache coherence protocol.

    b) Describe how multiport memories used in multistage networks.

    c) What is the use of reservation station ?

OR

16. a) Discuss the various instructions issue and completion policies with and without instruction look ahead in a superscalar processor.

    b) Describe data flow in hybrid architecture. **(3×20=60 Marks)**