Seventh Semester B.Tech. Degree Examination, October 2014
(2008 Scheme)
08.746 : LOW POWER VLSI DESIGN (TA)

Time : 3 Hours
Max. Marks : 100

Instructions: Answer all questions in Part – A. Each carries 4 marks. Answer any 2 questions from each Module in Part – B, each carries 10 marks.

PART – A

1. How can we reduce static power dissipation in CMOS circuits?

2. Explain basic principles of low power VLSI chips.

3. How does short circuit current in CMOS inverter vary with output capacitance?

4. Give the expressions showing the relation of static and conditional probabilities to transition probability and frequency in a lag one signal model.

5. How is leakage power dissipation related to transistor sizing?

6. Explain how equivalent pin ordering leads to better power efficiency.

7. Explain the concept of DETFF.

8. How does bus multiplexing improve power efficiency?

9. Explain any 2 methods to reduce power dissipation due to switching activities at architectural level.

10. Write a note on techniques for improving power efficiency in SRAM.

P.T.O.
PART – B
Module – 1

11. Explain the steps in Gate level power analysis using probabilistic approach.

12. Explain how stopping criteria is determined in Monte Carlo Simulation.

13. Explain the levels of abstraction in simulation based power estimation and explain how power analysis is done at architecture level.

Module – 2

14. Explain the concept of NPN equivalence in logic implementation. How digital cell library is optimized for a Boolean function using this concept?

15. Explain the concept of self gating FF and compare its power performance with regular FF.

16. Explain Precomputation logic. Derive the precomputation function for 
f(x1, x2, x3) = x1 x2 + x3.

Module – 3

17. Explain how parallelism and pipelining achieve low power dissipation at architectural level of abstraction.

18. Explain how control flow graph transformation is utilized in the design of low power DSP systems.

19. Give the concept of loop unrolling. Show how loop unrolling can be used to apply parallelism to the recursive computation structure given by
   \[ y(n) = x(n) + 3y(n-1). \]