PART – A

Answer all questions. Each question carries 4 marks.

1. Briefly explain the need for low power VLSI chips.

2. Explain charge sharing problems in dynamic circuits.

3. What is punch through? Why it must be prevented?

4. Compute transition density and static probability of \( y = a + bc \), \( P(a) = 0.5, P(b) = 0.4, P(c) = 0.1, D(a) = 2, D(b) = 1, D(c) = 3 \).

5. Explain how power reduction is achieved through gate sizing.

6. Explain transition analysis of state encoding.

7. Explain threshold voltage adjustment in low power devices.

8. Explain in brief recent trends in low power design for mobile application.

9. Explain how switching activity can be reduced in digital systems.

10. Explain DGD-ET-SOI.
PART – B

Answer any two questions from each Module. Each question carries 10 marks.

Module – I

11. Derive the expression for short circuit power dissipation of a CMOS inverter. Discuss short circuit current variations with load capacitance and input signal slope.

12. a) Explain the procedure of Monte Carlo power simulation.
    b) Briefly explain Gate level logic simulation.

13. Explain how power analysis is done for DSP systems.

Module – II

14. a) With the help of diagram explain two implementation of CMOS latches. Explain different trade off to be considered in the design.  
    b) Explain output Don’t care Encoding.

15. Analyse power consumption of SETFF and DETFF systems, with diagrams. Explain the disadvantage of DETFF.

16. Explain how power dissipation is reduced in off-chip buses.

Module – III

17. Explain in detail the low Power SRAM architecture.

18. Explain how control flow graph transformation improves power efficiency.

19. Explain in detail software power optimization.