(Pages : 2) 973

Reg. No. : .....

Name : .....

First Semester M.Tech. Degree Examination, March 2013
Computer Science and Engineering
RCC 1002 : COMPUTER ARCHITECTURE

Time : 3 Hours Max. Marks : 100

Answer **any five** questions.

1. a) Why are benchmark programs and benchmark suites used to measure computer performance ? 10

   b) When run on a given system, a program takes 1,00,000 cycles. If the system achieves a CPI of 40, how many instructions were executed in running the program ? 10

2. a) An unpipelined processor has a cycle time of 25 ns. What is the cycle time of a pipelined version of the processor with 5 evenly divided pipeline stages, if each pipeline latch has a latency of 1 ns ? What if the processor is divided into 50 pipeline stages. 10

   b) Why does pipelining improve performance ? 10

3. Use the following assembly code fragment :

I1 : ADDI $3, $0, 100	#$3 = 100
I2 : ADD $4, $0, $0	#$4 = 0
Loop :	
I3 : LW $5, 0($1)	#$5 = MEM [$1]
I4 : ADD $4, $4, $5	#$4 = $4 + $5
I5 : LW $6, 0($2)	#$6 = MEM[$2]
I6 : SUB $4, $4, $6	#$4 = $4 – $6
I7 : ADDI $1, $1, 4	#$1 = $1 + 4

P.T.O.

I8 : ADDI $2, $2, 4	#$2 = $2 + 4
I9 : ADDI $3, $3, –1	#$3 = $3 – 1
I10 : BNE $3, $0, Loop	if ($3 ! = 0) goto Loop

i) Show the timing of one loop iteration on the 5-stage pipeline processor without forwarding hardware. Complete the timing table, showing all the stall cycles. Assume that the branch will stall the pipeline for 1 clock cycle only.

ii) According to the timing diagram of part (i), Compute the number of clock cycles and the average CPI to execute ALL the iterations of the above loop.

iii) Reorder the instructions of the above loop to fill the load-delay and the branch delay slots, without changing the computation. Write the code of the modified loop. **(10+5+5)**

4. a) What is instruction-level parallelism ? How do processors exploit it to improve performance ? **10**

b) Describe about VLIM processors with a neat diagram. State the pros and cons of VLIM architecture. **10**

5. a) A program repeatedly executes a loop that has 120 iterations. Each iteration takes 10,000 cycles. On multiprocessor systems, 50,000 cycles are required to synchronize the processors once all iterations of the loop have completed. **10**

a) What is the execution time of each loop on a uniprocessor system ?

b) What is the execution time of each loop on a 2-processor system and what is the speedup over the uniprocessor system ?

c) What is the execution time of each loop on a 4-processor system and what is the speedup over the uniprocessor and 2-processor system ?

b) Explain the architecture of different multiprocessor systems. **10**

6. a) Draw the block diagram of a vector supercomputer and narrate about various units of the vector supercomputer. **10**

b) Write short notes on: i) Array processors ii) Systolic processors **(5+5)**