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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, December 2012
(2008 Scheme)
08.306 : DIGITAL ELECTRONICS (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. Convert the following numbers into decimal.
   a) $(121210.1210)_3$
   b) $(4321.414)_5$
2. Simplify $Y = AB + \overline{A}C + A\overline{B}C(AB + C)$.
3. Obtain the canonical POS form of expression
   $Y(A,B,C) = (A + \overline{B})\,(B + C)(A + .\overline{C})$.
4. Write down the applications of multiplexers.
5. Define :
   a) Noise margin
   b) Fanout of logic families.
6. Draw the state diagram of an SR flip flop.
7. Why preset and clear inputs of a flip flop is called asynchronous inputs ?
8. What is meant by an essential hazard ?
9. Define :
   a) Race
   b) Cycle.
10. Write a note on state reduction of sequential circuits. **(10×4=40 Marks)**

P.T.O.

PART – B

Answer **any two** questions from **each** Module.

Module – I

11. a) If $A\overline{B} + \overline{A}B = C$, show that $A\overline{C} + \overline{A}C = B$.

    b) Using Karnaugh map simplify the SOP function

    $f(a, b, c, d) = \Sigma(0, 1, 2, 4, 5, 6), d = \Sigma(3, 7, 14, 15)$.

12. Draw the truth table, logic diagram and circuit diagram of a 4 : 1 multiplexer.

13. Design a ripple carry adder. What is the limitation ? How the limitation is overcame in look ahead carry adder ?

Module – II

14. a) Draw the circuit diagram of a CMOS NAND gate, and explain the working.

    b) Compare TTL and CMOS logic families.

15. Explain the working of a universal shift register.

16. Design and explain the working of a Modulo 5 synchronous counter.

Module – III

17. a) Explain with the help of an example how a Moore machine is converted into a Mealy machine.

    b) Draw Moore and Mealy notations of a JK flip flop.

18. With the help of a state table and state diagram design a mod 5 up down counter.

19. Design a sequence detector to detect a sequence '110101' in a stream of bits.

(20×3=60 Marks)