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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, April/May 2012
(2008 Scheme)
Branch : ELECTRONICS AND COMMUNICATION ENGINEERING
08.306 : Digital Electronics (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. Using Boolean rules and laws, simplify

   $f = \bar{a}\,\bar{b}\,\bar{c} + \bar{a}\,\bar{b}c + a\bar{b}\,\bar{c} + abc$

2. Show how a full adder can be made to subtract.

3. Write VHDL program for NAND and NOR gates.

4. Explain a basic static RAM storage cell.

5. What are the input and output voltage levels of TTL ?

6. Define flip flop set up time and hold time with diagram.

7. Explain the differences between non retriggerable and retriggerable monostable multivibrators.

8. With an example, explain partial flow table showing a cycle in an asynchronous machine.

9. Distinguish between fundamental and pulse mode asynchronous sequential circuits.

10. Explain static, dynamic and essential hazards with examples.

P.T.O.

PART – B

Answer **any 2** questions from **each** Module. **Each** question carries **10** marks.

MODULE – 1

11. Using Quine Mc-Cluskey method, simplify the following Boolean function and design a circuit using NAND gates.

    $f(a, b, c, d) = \sum(0, 3, 4, 5, 6) + \sum d(1, 7, 10, 15)$

12. a) Using a 2 to 4 decoder, realise the Boolean function. $F = \overline{a}\,\overline{b} + ab$.

    b) Determine the ripple carry propagation delay for a 4 bit adder. Find the total average current requirement.

13. a) Realise a full adder using multiplexer.

    b) Realise $f = w\,\overline{y} + \overline{y}\,z$ using a 3 to 8 decoder.

MODULE – 2

14. a) Draw the internal circuit of a tristate TTL gate and explain its working.

    b) When a TTL gate drives 5 TTL inputs, find sinking current and sourcing current of driver.

15. Draw the circuit of a universal shift register and explain its working.

16. a) What are the flip flop timing specifications ?

    b) Design a Mod-6 synchronous counter with D flip flops.

MODULE – 3

17. a) Draw the Mealy and Moore sequential circuit models and explain the differences between them.

    b) Construct state diagram for a Mealy sequential circuit that will detect the serial input sequence $x = 010110$. When complete sequence has been detected then cause output z to go high.

18. Reduce the following state tables using the equivalence class state reduction technique.

Present state	Next state		Output	
	x = 0	x = 1	x = 0	x= 1
S_0	S_2	S_1	0	1
S_1	S_3	S_1	0	1
S_2	S_0	S_3	1	0
S_3	S_1	S_2	1	0

19.a) What are races and cycles ? Explain with example.

b) Design a hazard free combinational circuit $f = \sum m(0, 1, 2, 3, 10, 11, 15)$.