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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, November 2013
(2008 Scheme)
08.306 : DIGITAL ELECTRONICS (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions.

1. Write the entry declarations in VHDL to specify inputs and outputs of a full adder module.
2. Convert a T – flipflop into D – flipflop.
3. Represent the following functions on a K-map

   a) $Y = \overline{a}\, b\, c + a\, b\, \overline{c} + a\, b\, c + a\, b\, \overline{d}$

   b) $Y = AB + \overline{A}\,\overline{B}$.
4. Represent 2587_{10}

   a) in B C D

   b) in Hex

   c) in Excess three code.
5. Draw the Moore sequential model. How it differs from the Mealy machine ?
6. Compare TTL and ECL gates.
7. Define flow table in synchronous circuits.

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8. What is meant by static hazards ? Draw circuits with a static – I hazard and static – I hazard free.

9. How can a 74121 be configured as a monostable multivibrator for a described pulse width ?

10. Differentiate ring counter and twisted ring counter. **(10×4=40 Marks)**

PART – B

Answer **any two** questions from **each** Module. **Each** question carries **10** marks.

Module – I

11. Obtain minimal expression in SDP and POS forms for the boolean expression $S = \sum m(0, 1, 2, 5, 7, 9, 10)$. Use Karnaugh Map.

12. a) Realize a full adder using NAND gates only.

    b) Design a circuit that compares two 2 bit numbers P and Q and produce output bits that indicate whether P = Q of P > Q.

13. a) Implement the logic $S = \sum m(0, 1, 2, 5, 6)$ using an appropriate multiplexer.

    b) Draw the basic structure of a 16×4 ROM. Explain its operation.

Module – II

14. Design a counter using T – flip flop to count the following sequence

    0 – 3 – 1 – 4 – 6 – 0.

15. a) Design an astable multivibrator of frequency 1 KHz using NAND gates.

    b) Design a combinational circuit to determine the 2's complement of 4 – bit binary number.

16. Draw the circuit diagram of an ECL NOR/OR gate and explain its operation. Compare its performance with that of CMOS logic gate.

Module – III

17. A synchronous counter steers through the state sequence given by

    0, 1, 3, 2, 6, 7, 5, 4. Name the code and explain the process of its development. Design the counter using JK flip-flop.

18. A system with one input x and one output z such that z = 1 iff x has been 1' for at least 3 consecutive clock time. Implement using T – flip flop as a Mealy system.

19. Obtain a minimum row primitive flow table for the state table shown below :

(6×10=60 Marks)

	X_1X_2				
	00	01	11	10	Z_1Z_2
1	(1)	7	–	4	11
2	(2)	5	–	4	01
3	–	7	(3)	11	10
4	2	–	3	(4)	00
5	6	(5)	9	–	11
6	(6)	7	–	11	01
7	1	(7)	14	–	10
8	(8)	12	–	4	01
9	–	7	(9)	13	01
10	–	7	(10)	4	10
11	8	–	10	(11)	00
12	6	(12)	9	–	11
13	8	–	14	(13)	11
14	–	12	(14)	11	00

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