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Reg. No. : .....

Name : .....

Sixth Semester B.Tech. Degree Examination, May 2012
(2008 Scheme)
08.602 : VLSI DESIGN (TA)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. State Fick's laws of diffusion.
2. Why is Rapid Thermal annealing preferred over conventional furnace annealing ?
3. What are the different types of optical lithography ? Discuss advantages and disadvantages of each.
4. What is junction spiking ?
5. Implement a 4 : 1 mux using pass transistors.
6. Draw a 2 input NOR gate using CMOS logic and size each transistor to have same t_{PHL} and t_{PLH} as a static CMOS inverter.
7. Explain Drain Induced Barrier Lowering.
8. How are carry look ahead adder modules interconnected to get higher order adders ?
9. Explain the working of carry bypass adder.
10. Derive the expression for dynamic power dissipation of static CMOS inverter.

PART – B

Answer **two** questions from **each** Module. **(6×10=60 Marks)**

Module – I

11. Explain PN junction isolation. How are the disadvantages of PN junction isolation overcome using dielectric isolation.
12. Explain fabrication sequence of an n well CMOS with neat diagrams.
13. Explain CVD system for epitaxial growth.

P.T.O.

Module – II

14. Discuss constant field and constant voltage scaling. How are the drawbacks of these two scaling eliminated in generalized scaling ?

15. a) Draw VLSI design flow diagram and explain. **5**

    b) Discuss the concept of np logic. **5**

16. a) Explain charge sharing in dynamic logic. **5**

    b) Derive the square law model of I_D vs V_{DS} characteristics of a MOSFET. **5**

Module – III

17. a) Define the terms controllability, observability and fault coverage. **5**

    b) Describe how self-in built test is carried out. **5**

18. Show the CMOS implementation of a NOR ROM cell to store 4 words of 4 bits which are as follows 1011, 0110, 1001 and 1100. **10**

19. a) Explain the principle of a regester based multiplier. **5**

    b) How is booth encoding used to speed up multiplication process. **5**